SPECIFICATIONS

CIO-DAS802/16

Analog Input & Digital I/O

Revision 4, August, 2001

Power consumption

+5V quiescent	430 mA typical, 675 mA max

Analog input section

A/D converter type	AD7805PB, Successive-approximation
Resolution	16 bits
Number of channels	8
Input ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V, fully programmable
Polarity	Unipolar/Bipolar software-selectable, 11 ms max switching delay
A/D pacing	Programmable: internal counter or external source (IR Input / XCLK, falling edge) or software polled
A/D Trigger sources	External hardware (Digital In 1 / Trig, rising edge)
Data transfer	Interrupt or software polled from 256-sample FIFO buffer
Channel configuration	Differential (or pseudo-differential with installation of a SIP resistor) or single-ended, switch-selectable for each channel
DMA	None
A/D conversion time	10 µs (including signal acquisition time)
Throughput	100 kHz
Accuracy	±0.0015% of reading ±1.5 LSB
Differential Linearity error	+1.5/−1 LSB max
Integral Linearity error	±1.5 LSB max
No missing codes (guaranteed)	16 bits
Gain drift (A/D specs)	±10 ppm/°C
Zero drift (A/D specs)	±5 ppm/°C
Common Mode Range	±10V
CMRR @ 60 Hz	90 dB min
Input leakage current (@ 25°C)	100 nA
Input impedance	10 Mohms
Absolute max. input voltage	±35V

Counter section

Counter type	82C54
Configuration	3 down-counters , 16-bit resolution

Counter 0 - independent user counter
- Source: external, user connector (Counter 0 In)
- Gate: external, user connector (Gate 0)
- Output: user connector (Counter 0 Out)

Counter 1 - ADC Pacer Lower Divider or independent user counter
- Source: user connector (Counter 1 In) and optionally, Counter Out, selectable by software
- Gate: programmable, disabled or user connector (Gate 1)
- Output: user connector (Counter 1 Out) and optionally to A/D start convert, software selectable

Counter 2 - ADC Pacer Upper Divider
- Source: internal 1 MHz oscillator
- Gate: programmable, disabled or user connector (Gate 2)
- Output: user connector (Counter 2 Out) and optionally to Counter 1 input, software selectable

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Digital I/O section

Digital type	Input: FPGA Output: 74LS08
Configuration	Two ports, 3 input and 4 output
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage (IOL = 8 mA)	0.25V typical, 0.4V max
Output high voltage (OH = –0.4 mA)	3.4V typical, 2.7V min
Absolute maximum input voltage	–0.5V, +5.5V
Interrupts	Jumper selectable: levels 2, 3, 4, 5, 6, 7, or not connected Positive edge triggered
Interrupt enable	Programmable
Interrupt sources	External (IR Input / XCLK), A/D End-of-conversion, A/D FIFO-half-full

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing

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