

# Specifications

**PCI-DAS6071**



**MEASUREMENT  
COMPUTING™**

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# Specifications

Typical for 25°C unless otherwise specified.

## Analog Input Section

|                                 |                                                                                                                                                                                                                        |
|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A/D converter type              | Successive Approximation                                                                                                                                                                                               |
| Maximum Sample Rate             | 1.25MS/s                                                                                                                                                                                                               |
| Resolution                      | 12 bits, 1-in-4096                                                                                                                                                                                                     |
| Number of channels              | 64 single ended / 32 differential, Software selectable                                                                                                                                                                 |
| Input ranges                    | Bipolar: $\pm 10V$ , $\pm 5V$ , $\pm 2.5V$ , $\pm 1V$ , $\pm 0.5V$ , $\pm 0.25V$ , $\pm 0.1V$ , $\pm 0.05V$ ,<br>Unipolar: 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V, 0 to 0.1V<br>Software selectable |
| A/D pacing<br>(SW programmable) | Internal counter – ASIC. Software selectable time base: <ul style="list-style-type: none"><li>Internal 40MHz, 50ppm stability</li><li>External Source via AUXIN&lt;5:0&gt;, Software selectable.</li></ul>             |
|                                 | External convert strobe: A/D CONVERT                                                                                                                                                                                   |
|                                 | Software paced                                                                                                                                                                                                         |
| Burst mode                      | Software selectable option, burst rate = 800nS                                                                                                                                                                         |
| A/D Gate Sources                | External digital: A/D GATE                                                                                                                                                                                             |
|                                 | External analog: ATRIG input<br>CH0 IN through CH63 IN                                                                                                                                                                 |
| A/D gating modes                | External digital: Programmable, active high or active low, level or edge                                                                                                                                               |
|                                 | External analog:                                                                                                                                                                                                       |
| A/D trigger sources             | External digital: A/D START TRIGGER<br>A/D STOP TRIGGER                                                                                                                                                                |
|                                 | External analog: ATRIG input<br>CH0 IN through CH63 IN                                                                                                                                                                 |
| A/D triggering modes            | External digital: Software-configurable for rising or falling edge.                                                                                                                                                    |
|                                 | External analog: See Analog Trigger section                                                                                                                                                                            |
|                                 | Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.                                                                                                                               |
| ADC Pacer Out                   | Available at user connector: A/D PACER OUT                                                                                                                                                                             |
| RAM buffer size                 | 8K samples                                                                                                                                                                                                             |
| Data transfer                   | DMA                                                                                                                                                                                                                    |
|                                 | Programmed I/O                                                                                                                                                                                                         |
| DMA Modes                       | Demand or Non-Demand using scatter gather.                                                                                                                                                                             |
| Configuration Memory            | Up to 8K elements. Programmable channel, gain, and offset                                                                                                                                                              |
| Streaming-to-disk rate          | 1.25MS/s, system dependent                                                                                                                                                                                             |

## Accuracy

1.25 MS/s rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within  $\pm 1^{\circ}\text{C}$  of internal calibration temperature and  $\pm 10^{\circ}\text{C}$  of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 1 – Absolute Accuracy

| Range              | Absolute Accuracy (LSB) |
|--------------------|-------------------------|
| $\pm 10\text{V}$   | $\pm 2.9$               |
| $\pm 5\text{V}$    | $\pm 2.1$               |
| $\pm 2.5\text{V}$  | $\pm 3.0$               |
| $\pm 1\text{V}$    | $\pm 3.0$               |
| $\pm 500\text{mV}$ | $\pm 3.0$               |
| $\pm 250\text{mV}$ | $\pm 3.1$               |
| $\pm 100\text{mV}$ | $\pm 3.3$               |
| $\pm 50\text{mV}$  | $\pm 3.7$               |
| 0 to 10V           | $\pm 2.8$               |
| 0 to 5V            | $\pm 4.4$               |
| 0 to 2V            | $\pm 4.4$               |
| 0 to 1V            | $\pm 4.5$               |
| 0 to 500mV         | $\pm 4.6$               |
| 0 to 200mV         | $\pm 4.8$               |
| 0 to 100mV         | $\pm 5.2$               |

Table 2 – Absolute Accuracy components - All values are ( $\pm$ )

| Range              | % of Reading | Offset (mV) | Noise + Quantization (mV) |                       | Temp Drift (%/DegC) | Absolute Accuracy at FS (mV) |
|--------------------|--------------|-------------|---------------------------|-----------------------|---------------------|------------------------------|
|                    |              |             | Single Pt                 | Averaged <sup>1</sup> |                     |                              |
| $\pm 10\text{V}$   | 0.0714       | 6.38        | 6.10                      | 0.846                 | 0.0010              | 14.369                       |
| $\pm 5\text{V}$    | 0.0314       | 3.20        | 3.05                      | 0.423                 | 0.0005              | 5.193                        |
| $\pm 2.5\text{V}$  | 0.0714       | 1.61        | 1.53                      | 0.211                 | 0.0010              | 3.605                        |
| $\pm 1\text{V}$    | 0.0714       | 0.653       | 0.610                     | 0.085                 | 0.0010              | 1.452                        |
| $\pm 500\text{mV}$ | 0.0714       | 0.335       | 0.305                     | 0.042                 | 0.0010              | 0.735                        |
| $\pm 250\text{mV}$ | 0.0714       | 0.176       | 0.208                     | 0.024                 | 0.0010              | 0.379                        |
| $\pm 100\text{mV}$ | 0.0714       | 0.081       | 0.098                     | 0.011                 | 0.0010              | 0.163                        |
| $\pm 50\text{mV}$  | 0.0714       | 0.049       | 0.071                     | 0.007                 | 0.0010              | 0.091                        |
| 0 to 10V           | 0.0314       | 3.20        | 3.05                      | 0.423                 | 0.0005              | 6.765                        |
| 0 to 5V            | 0.0714       | 1.61        | 1.53                      | 0.211                 | 0.0010              | 5.391                        |
| 0 to 2V            | 0.0714       | 0.653       | 0.610                     | 0.085                 | 0.0010              | 2.167                        |
| 0 to 1V            | 0.0714       | 0.335       | 0.305                     | 0.042                 | 0.0010              | 1.092                        |

| Range      | % of Reading | Offset (mV) | Noise + Quantization (mV) |                       | Temp Drift (%/DegC) | Absolute Accuracy at FS (mV) |
|------------|--------------|-------------|---------------------------|-----------------------|---------------------|------------------------------|
|            |              |             | Single Pt                 | Averaged <sup>1</sup> |                     |                              |
| 0 to 500mV | 0.0714       | 0.176       | 0.208                     | 0.024                 | 0.0010              | 0.558                        |
| 0 to 200mV | 0.0714       | 0.081       | 0.098                     | 0.011                 | 0.0010              | 0.235                        |
| 0 to 100mV | 0.0714       | 0.049       | 0.071                     | 0.007                 | 0.0010              | 0.127                        |

1. Averaged measurements assume dithering and averaging of 100 single-channel readings.

Each PCI-DAS6071 is tested at the factory to assure the board's overall error does not exceed absolute accuracy limits described in [Table 1](#) on page 2.

Table 3 – Relative Accuracy - All values are ( $\pm$ )

| Range       | Relative Accuracy (mV) |                       |
|-------------|------------------------|-----------------------|
|             | Single Point           | Averaged <sup>1</sup> |
| $\pm 10V$   | 7.37                   | 1.11                  |
| $\pm 5V$    | 3.68                   | 0.557                 |
| $\pm 2.5V$  | 1.84                   | 0.278                 |
| $\pm 1V$    | 0.737                  | 0.111                 |
| $\pm 500mV$ | 0.368                  | 0.056                 |
| $\pm 250mV$ | 0.238                  | 0.032                 |
| $\pm 100mV$ | 0.111                  | 0.015                 |
| $\pm 50mV$  | 0.082                  | 0.009                 |
| 0 to 10V    | 3.68                   | 0.557                 |
| 0 to 5V     | 1.84                   | 0.278                 |
| 0 to 2V     | 0.737                  | 0.111                 |
| 0 to 1V     | 0.368                  | 0.056                 |
| 0 to 500mV  | 0.238                  | 0.032                 |
| 0 to 200mV  | 0.111                  | 0.015                 |
| 0 to 100mV  | 0.082                  | 0.009                 |

1. Averaged measurements assume dithering and averaging of 100 single-channel readings.

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 4 – Differential non-linearity

|            |                   |                   |
|------------|-------------------|-------------------|
| All Ranges | $\pm 0.5$ LSB typ | $\pm 1.0$ LSB max |
|------------|-------------------|-------------------|

## Settling Time

Settling time is defined here as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at a specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

| Condition                | Range       | Accuracy   |                                   |                                   |                                   |
|--------------------------|-------------|------------|-----------------------------------|-----------------------------------|-----------------------------------|
|                          |             |            | $\pm 0.012\%$<br>( $\pm 0.5$ LSB) | $\pm 0.024\%$<br>( $\pm 1.0$ LSB) | $\pm 0.098\%$<br>( $\pm 4.0$ LSB) |
| Same range to same range | $\pm 10V$   | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.9 $\mu$ S<br>2.0 $\mu$ S        |
|                          | $\pm 5V$    | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.5 $\mu$ S        |
|                          | $\pm 2.5V$  | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | $\pm 1V$    | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | $\pm 500mV$ | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | $\pm 250mV$ | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | $\pm 100mV$ | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | $\pm 50mV$  | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.5 $\mu$ S        |
|                          |             |            |                                   |                                   |                                   |
|                          | 0 to 10V    | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.5 $\mu$ S        |
|                          | 0 to 5V     | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | 0 to 2V     | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | 0 to 1V     | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | 0 to 500mV  | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | 0 to 200mV  | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.3 $\mu$ S        |
|                          | 0 to 100mV  | Typ<br>Max | 3.0 $\mu$ S<br>5.0 $\mu$ S        | 1.9 $\mu$ S<br>2.5 $\mu$ S        | 1.2 $\mu$ S<br>1.5 $\mu$ S        |

## Parametrics

|                                            |                                                                                               |        |
|--------------------------------------------|-----------------------------------------------------------------------------------------------|--------|
| Max working voltage (signal + common-mode) | Input must remain within $\pm 11\text{V}$ of ground                                           |        |
| CMRR @ 60Hz                                | $\pm 10\text{V}$                                                                              | 95 dB  |
|                                            | $\pm 5\text{V}$ , 0 to 10V                                                                    | 100 dB |
|                                            | All other ranges                                                                              | 106 dB |
| Small signal bandwidth, all ranges         | 1.6 MHz                                                                                       |        |
| Large signal bandwidth, all ranges         | 1.0 MHz                                                                                       |        |
| Input coupling                             | DC                                                                                            |        |
| Input impedance                            | 100 Gohm in parallel with 100pF in normal operation.                                          |        |
|                                            | 820 Ohm in powered off or overload condition.                                                 |        |
| Input bias current                         | $\pm 200\text{pA}$                                                                            |        |
| Input offset current                       | $\pm 100\text{pA}$                                                                            |        |
| Absolute maximum input voltage             | $\pm 25$ power on, $\pm 15\text{V}$ power off. Protected Inputs:                              |        |
|                                            | <ul style="list-style-type: none"> <li>▪ CH0 IN through CH63 IN</li> <li>▪ AISENSE</li> </ul> |        |
| Crosstalk, DC to 100kHz                    | Adjacent Channels: -75dB                                                                      |        |
|                                            | All other Channels: -90dB                                                                     |        |

## Noise Performance

Table 5 below summarizes the noise performance for the PCI-DAS6071. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 5 – Analog Input Noise Performance (not including quantization)

| Range              | Counts Dithered | LSBrms Dithered | Counts Undithered | LSBrms Undithered |
|--------------------|-----------------|-----------------|-------------------|-------------------|
| $\pm 10\text{V}$   | 5               | 0.5             | 3                 | 0.25              |
| $\pm 5\text{V}$    | 5               | 0.5             | 3                 | 0.25              |
| $\pm 2.5\text{V}$  | 5               | 0.5             | 3                 | 0.25              |
| $\pm 1\text{V}$    | 5               | 0.5             | 3                 | 0.25              |
| $\pm 500\text{mV}$ | 6               | 0.5             | 3                 | 0.25              |
| $\pm 250\text{mV}$ | 6               | 0.6             | 4                 | 0.4               |
| $\pm 100\text{mV}$ | 7               | 0.7             | 5                 | 0.5               |
| $\pm 50\text{mV}$  | 9               | 0.9             | 8                 | 0.8               |
|                    |                 |                 |                   |                   |
| 0 to 10V           | 5               | 0.5             | 3                 | 0.25              |
| 0 to 5V            | 5               | 0.5             | 3                 | 0.25              |
| 0 to 2V            | 5               | 0.5             | 3                 | 0.25              |
| 0 to 1V            | 6               | 0.5             | 3                 | 0.25              |

| Range      | Counts Dithered | LSBrms Dithered | Counts Undithered | LSBrms Undithered |
|------------|-----------------|-----------------|-------------------|-------------------|
| 0 to 500mV | 6               | 0.6             | 4                 | 0.4               |
| 0 to 200mV | 7               | 0.7             | 5                 | 0.5               |
| 0 to 100mV | 9               | 0.9             | 8                 | 0.8               |

## Analog Output Section

|                                                              |                                                               |
|--------------------------------------------------------------|---------------------------------------------------------------|
| D/A Converter type                                           | Double-buffered, multiplying                                  |
| Resolution                                                   | 12-bits, 1-in-4096                                            |
| Number of Channels                                           | 2 voltage output                                              |
| Voltage Range                                                | ±10V, 0 to 10V, ±EXT REF., 0 to EXT REF., software selectable |
| Monotonicity                                                 | 12-bits, guaranteed                                           |
| Slew Rate                                                    | 20V/μs min                                                    |
| Settling Time (full scale step)                              | 3.0μs to ±0.5 LSB accuracy                                    |
| Noise                                                        | 200μVrms, DC to 1MHz BW                                       |
| Glitch Energy                                                | ±20mV @ 1.5μs duration measured at mid-scale transition.      |
| Current Drive                                                | ±5 mA                                                         |
| Output short-circuit duration                                | Indefinite @25mA                                              |
| Output coupling                                              | DC                                                            |
| Output impedance                                             | 0.1 ohms max                                                  |
| Gain temperature coefficient, internal or external reference | 25ppm/°C                                                      |
| Offset temperature coefficient                               | ±50μV/°C                                                      |
| Power up and reset                                           | DACs cleared to 0 volts ±200mV max                            |

Table 6 – Analog Output Absolute Accuracy

| Range    | Absolute Accuracy (LSB) |
|----------|-------------------------|
| ±10V     | ±1.7 LSB                |
| 0 to 10V | ±2.3 LSB                |

Table 7 – Analog Output Absolute Accuracy Components

| Range    | % of Reading | Offset (mV) | Temp Drift (%/DegC) | Absolute Accuracy at FS (mV) |
|----------|--------------|-------------|---------------------|------------------------------|
| ±10V     | ±0.0219      | ±5.93       | ±0.0005             | ±8.127                       |
| 0 to 10V | ±0.0219      | ±3.49       | ±0.0005             | ±5.685                       |

Each PCI-DAS6071 is tested at the factory to assure the board's overall error does not exceed the limits listed in *Table 6* above.

Table 8 – Relative Accuracy

| Range      | Relative Accuracy |               |
|------------|-------------------|---------------|
| All Ranges | ±0.3 LSB, typical | ±0.5 LSB, max |

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Table 9 – Differential non-linearity

|            |                        |                    |
|------------|------------------------|--------------------|
| All Ranges | $\pm 0.3$ LSB, typical | $\pm 1.0$ LSB, max |
|------------|------------------------|--------------------|

### Analog Output Pacing and Triggering

|                                            |                                                                                                                                                           |
|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| DAC pacing<br>(SW programmable)            | Internal counter – ASIC. Selectable time base:                                                                                                            |
|                                            | <ul style="list-style-type: none"> <li>▪ Internal 40MHz</li> <li>▪ External Source via AUXIN&lt;5:0&gt;, SW selectable.</li> </ul>                        |
|                                            | External convert strobe: D/A UPDATE                                                                                                                       |
|                                            | Software paced                                                                                                                                            |
| DAC Gate Source<br>(Software programmable) | External digital: D/A START TRIGGER                                                                                                                       |
|                                            | External analog: ATRIG input<br>CH0 IN through CH63 IN                                                                                                    |
|                                            | Software gated                                                                                                                                            |
| DAC gating modes                           | External digital:                                                                                                                                         |
|                                            | Programmable, active high or active low, level or edge<br><ul style="list-style-type: none"> <li>• External analog: See Analog Trigger section</li> </ul> |
| DAC trigger sources                        | External digital: D/A START TRIGGER                                                                                                                       |
|                                            | External analog: ATRIG input<br>CH0 IN through CH63 IN                                                                                                    |
|                                            | Software triggered                                                                                                                                        |

|                                |                                                                     |
|--------------------------------|---------------------------------------------------------------------|
| DAC triggering modes           | External digital: Software-configurable for rising or falling edge. |
|                                | External analog: See Analog Trigger section                         |
| DAC pacer Out                  | Available at user connector: D/A PACER OUT                          |
| RAM Buffer Size                | 16K samples                                                         |
| Data transfer                  | DMA                                                                 |
|                                | Programmed I/O                                                      |
|                                | Update DACs individually or simultaneously, software selectable.    |
| DMA Modes                      | Demand or Non-Demand using scatter gather.                          |
| Waveform generation throughput | 1 MS/s max per channel, 2 channels simultaneous                     |

### Analog Output External Reference Input (D/A EXTREF)

|                          |                                               |
|--------------------------|-----------------------------------------------|
| Range                    | $\pm 11$ V                                    |
| Overvoltage Protection   | $\pm 25$ V powered on, $\pm 15$ V powered off |
| Input Impedance          | 10k ohms                                      |
| Bandwidth (-3dB)         | 1 MHz                                         |
| Gain Error – EXTREF mode | 0 to 0.5%, not adjustable.                    |

## Analog Trigger

|                                               |                                                                                                                                         |         |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------|
| Analog Trigger Sources<br>Software selectable | External: ATRIG input<br>CH0 IN through CH63 IN, first channel in scan                                                                  |         |
| Analog Trigger Levels                         | ATRIG input: $\pm 10V$                                                                                                                  |         |
|                                               | CH0 IN through CH63 IN: $\pm$ Full-scale, range dependent                                                                               |         |
| Analog Trigger Modes                          | External analog: Software-configurable for:<br>▪ Positive or Negative slope                                                             |         |
| Analog Gate Modes                             | External analog: Software-configurable for:<br>▪ Above or Below reference<br>▪ Positive or Negative hysteresis<br>▪ In or Out of window |         |
| Resolution                                    | 8-bits, 1-in-256                                                                                                                        |         |
| Accuracy                                      | $\pm 5\%$ Full-scale range max                                                                                                          |         |
| Bandwidth (-3dB)                              | ATRIG input                                                                                                                             | 1.3 MHz |
|                                               | CH0 IN through CH63 IN                                                                                                                  | 2.0 MHz |

## Analog Input / Output Calibration

|                               |                                                                                           |
|-------------------------------|-------------------------------------------------------------------------------------------|
| Recommended warm-up time      | 15 minutes                                                                                |
| Calibration                   | Auto-calibration, calibration factors for each range stored on board in non-volatile RAM. |
| Onboard calibration reference | DC Level: $5.000V \pm 2.5mv$ . Actual measured values stored in EEPROM.                   |
|                               | Tempco: 5ppm/ $^{\circ}C$ max, 2ppm/ $^{\circ}C$ typical                                  |
|                               | Long-term stability: 20ppm, T = 1000 hrs, non-cumulative                                  |
| Calibration interval          | 1 year                                                                                    |

## Digital Input / Output

|                                   |                                                                                                                                                                                                 |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Digital Type                      | Discrete, 5V/TTL compatible                                                                                                                                                                     |
| Number of I/O                     | 8                                                                                                                                                                                               |
| Configuration                     | 8 bits, independently programmable for input or output. All pins pulled up to +5V via 47K resistors (default). Positions available for pull down to ground. Hardware selectable via solder gap. |
| Input high voltage                | 2.0V min, 7.0V absolute max                                                                                                                                                                     |
| Input low voltage                 | 0.8V max, -0.5V absolute min                                                                                                                                                                    |
| Output high voltage (IOH = -32mA) | 3.80V min, 4.20V typ                                                                                                                                                                            |
| Output low voltage (IOL = 32mA)   | 0.55V max, 0.22V typ                                                                                                                                                                            |
| Data Transfer                     | Programmed I/O                                                                                                                                                                                  |
| Power-up / reset state            | Input mode (high impedance)                                                                                                                                                                     |

## Interrupt Section

|                                                  |                                                                                                |
|--------------------------------------------------|------------------------------------------------------------------------------------------------|
| Interrupts                                       | PCI INTA# - mapped to IRQn via PCI BIOS at boot-time                                           |
| Interrupt enable                                 | Programmable through PLX9080                                                                   |
| ADC Interrupt sources<br>(Software Programmable) | DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.                              |
|                                                  | DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.                         |
|                                                  | DAQ_DONE: Interrupt is generated when a DAQ sequence completes.                                |
|                                                  | DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is 1/4 full.                           |
|                                                  | DAQ_SINGLE: Interrupt is generated after each conversion completes.                            |
|                                                  | DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans. |
|                                                  | DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.        |
| DAC Interrupt sources<br>(Software Programmable) | DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.                      |
|                                                  | DAC_DONE: Interrupt is generated when a DAC sequence completes.                                |
|                                                  | DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is 1/4 empty.                              |
|                                                  | DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.          |

## Counter Section

|                                              |                                                                  |
|----------------------------------------------|------------------------------------------------------------------|
| User counter type                            | 82C54                                                            |
| Number of Channels                           | 2                                                                |
| Resolution                                   | 16-bits                                                          |
| Compatibility                                | 5V/TTL                                                           |
| CTRn base clock source (Software selectable) | Internal 10MHz, Internal 100kHz or External connector (CTRn CLK) |
| Internal 10MHz clock source stability        | 50ppm                                                            |
| Counter n Gate                               | Available at connector (CTRn GATE).                              |
| Counter n Output                             | Available at connector (CTRn OUT).                               |
| Clock input frequency                        | 10 MHz max                                                       |
| High pulse width (clock input)               | 15ns min                                                         |
| Low pulse width (clock input)                | 25ns min                                                         |
| Gate width high                              | 25ns min                                                         |
| Gate width low                               | 25ns min                                                         |
| Input low voltage                            | 0.8V max                                                         |
| Input high voltage                           | 2.0V min                                                         |
| Output low voltage                           | 0.4V max                                                         |
| Output high voltage                          | 3.0V min                                                         |

## Configurable AUXIN<5:0>, AUXOUT<2:0> External Trigger/Clocks

The PCI-DAS6071 provides nine user-configurable Trigger/Clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

|                                        |                                             |                                                                              |
|----------------------------------------|---------------------------------------------|------------------------------------------------------------------------------|
| AUXIN<5:0> Sources<br>(SW selectable)  | A/D CONVERT:                                | External ADC convert strobe                                                  |
|                                        | A/D TIMEBASE IN:                            | External ADC pacer timebase                                                  |
|                                        | A/D START TRIGGER:                          | ADC Start Trigger                                                            |
|                                        | A/D STOP TRIGGER:                           | ADC Stop Trigger                                                             |
|                                        | A/D PACER GATE:                             | External ADC gate                                                            |
|                                        | D/A START TRIGGER:                          | DAC trigger/gate                                                             |
|                                        | D/A UPDATE:                                 | DAC update strobe                                                            |
|                                        | D/A TIMEBASE IN:                            | External DAC pacer time base                                                 |
| AUXOUT<2:0> Sources<br>(SW selectable) | STARTSCAN:                                  | A pulse indicating start of conversion                                       |
|                                        | SSH:                                        | Active signal that terminates at the start of the last conversion in a scan. |
|                                        | A/D STOP:                                   | Indicates end of scan                                                        |
|                                        | A/D CONVERT:                                | ADC convert pulse                                                            |
|                                        | SCANCLK:                                    | Delayed version of ADC convert                                               |
|                                        | CTR1 CLK                                    | CTR1 clock source                                                            |
|                                        | D/A UPDATE                                  | D/A update pulse                                                             |
|                                        | CTR2 CLK                                    | CTR2 clock source                                                            |
|                                        | A/D START TRIGGER:                          | ADC Start Trigger Out                                                        |
|                                        | A/D STOP TRIGGER:                           | ADC Stop Trigger Out                                                         |
| Default Selections:                    | AUXIN0:                                     | A/D CONVERT                                                                  |
|                                        | AUXIN1:                                     | A/D START TRIGGER                                                            |
|                                        | AUXIN2:                                     | A/D STOP TRIGGER                                                             |
|                                        | AUXIN3:                                     | D/A UPDATE                                                                   |
|                                        | AUXIN4:                                     | D/A START TRIGGER                                                            |
|                                        | AUXIN5:                                     | A/D PACER GATE                                                               |
|                                        | AUXOUT0:                                    | D/A UPDATE                                                                   |
|                                        | AUXOUT1:                                    | A/D CONVERT                                                                  |
|                                        | AUXOUT2:                                    | SCANCLK                                                                      |
| Compatibility                          | 5V/TTL                                      |                                                                              |
| Edge-sensitive polarity                | Rising/falling, software selectable         |                                                                              |
| Level-sensitive polarity               | Active high/active low, software selectable |                                                                              |
| Minimum pulse width                    | 37.5nS                                      |                                                                              |

## DAQ-Sync inter-board Triggers/Clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

|                   |                      |
|-------------------|----------------------|
| DAQ-Sync Signals: | DS A/D START TRIGGER |
|                   | DS A/D STOP TRIGGER  |
|                   | DS A/D CONVERT       |
|                   | DS D/A UPDATE        |
|                   | DS D/A START TRIGGER |
|                   | SYNC CLK             |

## Power Consumption

|                                |                                                                                      |
|--------------------------------|--------------------------------------------------------------------------------------|
| +5V                            | 0.9 A typical, 1.1 A max. Does not include power consumed through the I/O connector. |
| +5V available at I/O connector | 1A max, protected with a resettable fuse                                             |

## Environmental

|                             |                         |
|-----------------------------|-------------------------|
| Operating Temperature Range | 0 to 55°C               |
| Storage Temperature Range   | -20 to 70°C             |
| Humidity                    | 0 to 90% non-condensing |

## Mechanical

|                 |                                                     |
|-----------------|-----------------------------------------------------|
| Card dimensions | PCI half card: 174.6mm(L) x 106.9mm(W) x 11.65mm(H) |
|-----------------|-----------------------------------------------------|

## DAQ-Sync Connector and Pin Out

|                   |                                                                      |
|-------------------|----------------------------------------------------------------------|
| Connector type    | 14-Pin right-angle 100mil box header                                 |
| Compatible Cables | MCC p/n: CDS-14-x, 14 pin ribbon cable. x = number of boards (2 - 5) |

| Pin | Signal Name          |
|-----|----------------------|
| 1   | DS A/D START TRIGGER |
| 2   | GND                  |
| 3   | DS A/D STOP TRIGGER  |
| 4   | GND                  |
| 5   | DS A/D CONVERT       |
| 6   | GND                  |
| 7   | DS D/A UPDATE        |
| 8   | GND                  |
| 9   | DS D/A START TRIGGER |
| 10  | GND                  |
| 11  | RESERVED             |
| 12  | GND                  |
| 13  | SYNC CLK             |
| 14  | GND                  |

## Main Connector and Pin Out

|                                                           |                                                                                           |
|-----------------------------------------------------------|-------------------------------------------------------------------------------------------|
| Connector type                                            | Shielded SCSI 100 D-Type                                                                  |
| Compatible Cables                                         | C100HD50-x, unshielded ribbon cable. x= 3 or 6 feet                                       |
|                                                           | C100MMS-x, shielded round cable. x= 1, 2, or 3 meters                                     |
| Compatible accessory products<br>(with C100HD50-xx cable) | ISO-RACK16/P<br>ISO-DA02/P<br>BNC-16SE<br>BNC-16DI<br>CIO-MINI50<br>CIO-TERM100<br>SCB-50 |
| Compatible accessory products<br>(with C100MMS-x cable)   | SCB-100                                                                                   |

## 32 Channel Differential Mode

| Pin | Signal Name                  | Pin | Signal Name |
|-----|------------------------------|-----|-------------|
| 1   | LLGND                        | 51  | LLGND       |
| 2   | CH0 IN HI                    | 52  | CH16 IN HI  |
| 3   | CH0 IN LO                    | 53  | CH16 IN LO  |
| 4   | CH1 IN HI                    | 54  | CH17 IN HI  |
| 5   | CH1 IN LO                    | 55  | CH17 IN LO  |
| 6   | CH2 IN HI                    | 56  | CH18 IN HI  |
| 7   | CH2 IN LO                    | 57  | CH18 IN LO  |
| 8   | CH3 IN HI                    | 58  | CH19 IN HI  |
| 9   | CH3 IN LO                    | 59  | CH19 IN LO  |
| 10  | CH4 IN HI                    | 60  | CH20 IN HI  |
| 11  | CH4 IN LO                    | 61  | CH20 IN LO  |
| 12  | CH5 IN HI                    | 62  | CH21 IN HI  |
| 13  | CH5 IN LO                    | 63  | CH21 IN LO  |
| 14  | CH6 IN HI                    | 64  | CH22 IN HI  |
| 15  | CH6 IN LO                    | 65  | CH22 IN LO  |
| 16  | CH7 IN HI                    | 66  | CH23 IN HI  |
| 17  | CH7 IN LO                    | 67  | CH23 IN LO  |
| 18  | LLGND                        | 68  | LLGND       |
| 19  | CH8 IN HI                    | 69  | CH24 IN HI  |
| 20  | CH8 IN LO                    | 70  | CH24 IN LO  |
| 21  | CH9 IN HI                    | 71  | CH25 IN HI  |
| 22  | CH9 IN LO                    | 72  | CH25 IN LO  |
| 23  | CH10 IN HI                   | 73  | CH26 IN HI  |
| 24  | CH10 IN LO                   | 74  | CH26 IN LO  |
| 25  | CH11 IN HI                   | 75  | CH27 IN HI  |
| 26  | CH11 IN LO                   | 76  | CH27 IN LO  |
| 27  | CH12 IN HI                   | 77  | CH28 IN HI  |
| 28  | CH12 IN LO                   | 78  | CH28 IN LO  |
| 29  | CH13 IN HI                   | 79  | CH29 IN HI  |
| 30  | CH13 IN LO                   | 80  | CH29 IN LO  |
| 31  | CH14 IN HI                   | 81  | CH30 IN HI  |
| 32  | CH14 IN LO                   | 82  | CH30 IN LO  |
| 33  | CH15 IN HI                   | 83  | CH31 IN HI  |
| 34  | CH15 IN LO                   | 84  | CH31 IN LO  |
| 35  | AISENSE                      | 85  | DIO0        |
| 36  | D/A OUT 0                    | 86  | DIO1        |
| 37  | D/A GND                      | 87  | DIO2        |
| 38  | D/A OUT1                     | 88  | DIO3        |
| 39  | PC +5 V                      | 89  | DIO4        |
| 40  | AUXOUT0 / D/A PACER OUT      | 90  | DIO5        |
| 41  | AUXOUT1 / A/D PACER OUT      | 91  | DIO6        |
| 42  | AUXOUT2 / SCANCLK            | 92  | DIO7        |
| 43  | AUXIN0 / A/D CONVERT / ATRIG | 93  | CTR1 CLK    |
| 44  | D/A EXTREF                   | 94  | CTR1 GATE   |
| 45  | AUXIN1 / A/D START TRIGGER   | 95  | CTR1 OUT    |
| 46  | AUXIN2 / A/D STOP TRIGGER    | 96  | GND         |
| 47  | AUXIN3 / D/A UPDATE          | 97  | CTR2 CLK    |
| 48  | AUXIN4 / D/A START TRIGGER   | 98  | CTR2 GATE   |
| 49  | AUXIN5 / A/D PACER GATE      | 99  | CTR2 OUT    |
| 50  | GND                          | 100 | GND         |

## 64 Channel Single-Ended Mode

| Pin | Signal Name                  | Pin | Signal Name |
|-----|------------------------------|-----|-------------|
| 1   | LLGND                        | 51  | LLGND       |
| 2   | CH0 IN                       | 52  | CH16 IN     |
| 3   | CH32 IN                      | 53  | CH48 IN     |
| 4   | CH1 IN                       | 54  | CH17 IN     |
| 5   | CH33 IN                      | 55  | CH49 IN     |
| 6   | CH2 IN                       | 56  | CH18 IN     |
| 7   | CH34 IN                      | 57  | CH50 IN     |
| 8   | CH3 IN                       | 58  | CH19 IN     |
| 9   | CH35 IN                      | 59  | CH51 IN     |
| 10  | CH4 IN                       | 60  | CH20 IN     |
| 11  | CH36 IN                      | 61  | CH52 IN     |
| 12  | CH5 IN                       | 62  | CH21 IN     |
| 13  | CH37 IN                      | 63  | CH53 IN     |
| 14  | CH6 IN                       | 64  | CH22 IN     |
| 15  | CH38 IN                      | 65  | CH54 IN     |
| 16  | CH7 IN                       | 66  | CH23 IN     |
| 17  | CH39 IN                      | 67  | CH55 IN     |
| 18  | LLGND                        | 68  | LLGND       |
| 19  | CH8 IN                       | 69  | CH24 IN     |
| 20  | CH40 IN                      | 70  | CH56 IN     |
| 21  | CH9 IN                       | 71  | CH25 IN     |
| 22  | CH41 IN                      | 72  | CH57 IN     |
| 23  | CH10 IN                      | 73  | CH26 IN     |
| 24  | CH42 IN                      | 74  | CH58 IN     |
| 25  | CH11 IN                      | 75  | CH27 IN     |
| 26  | CH43 IN                      | 76  | CH59 IN     |
| 27  | CH12 IN                      | 77  | CH28 IN     |
| 28  | CH44 IN                      | 78  | CH60 IN     |
| 29  | CH13 IN                      | 79  | CH29 IN     |
| 30  | CH45 IN                      | 80  | CH61 IN     |
| 31  | CH14 IN                      | 81  | CH30 IN     |
| 32  | CH46 IN                      | 82  | CH62 IN     |
| 33  | CH15 IN                      | 83  | CH31 IN     |
| 34  | CH47 IN                      | 84  | CH63 IN     |
| 35  | AISENSE                      | 85  | DIO0        |
| 36  | D/A OUT 0                    | 86  | DIO1        |
| 37  | D/A GND                      | 87  | DIO2        |
| 38  | D/A OUT1                     | 88  | DIO3        |
| 39  | PC +5 V                      | 89  | DIO4        |
| 40  | AUXOUT0 / D/A PACER OUT      | 90  | DIO5        |
| 41  | AUXOUT1 / A/D PACER OUT      | 91  | DIO6        |
| 42  | AUXOUT2 / SCANCLK            | 92  | DIO7        |
| 43  | AUXIN0 / A/D CONVERT / ATRIG | 93  | CTR1 CLK    |
| 44  | D/A EXTREF                   | 94  | CTR1 GATE   |
| 45  | AUXIN1 / A/D START TRIGGER   | 95  | CTR1 OUT    |
| 46  | AUXIN2 / A/D STOP TRIGGER    | 96  | GND         |
| 47  | AUXIN3 / D/A UPDATE          | 97  | CTR2 CLK    |
| 48  | AUXIN4 / D/A START TRIGGER   | 98  | CTR2 GATE   |
| 49  | AUXIN5 / A/D PACER GATE      | 99  | CTR2 OUT    |
| 50  | GND                          | 100 | GND         |

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