

Specifications

PCI-DAS6023 & PCI-DAS6025



**MEASUREMENT
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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input section

Table 1. Analog input specifications

A/D converter type	Successive approximation type, min 200 kS/s conversion rate.
Resolution	12 bits, 1-in-4096
Number of channels	16 single ended / 8 differential. Software selectable
Input ranges	± 10 V, ± 5 V, ± 500 mV, ± 50 mV. Software selectable
A/D pacing (SW programmable)	Internal counter – ASIC. Software selectable time base: Internal 40 MHz, 50 ppm stability
	External source via AUXIN<5:0>. Software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 5 μ S.
A/D gate sources	External digital: A/D GATE
A/D gating modes	External digital: Programmable, active high or active low, level or edge
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 k samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or Non-Demand using scatter gather.
Configuration memory	Up to 8 k elements. Programmable channel, gain, and offset
Streaming-to-disk rate	200 kS/s, system dependent

Accuracy

200 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ± 1 °C of internal calibration temperature, and ± 10 °C of factory calibration temperature. Calculations for *Absolute Accuracy* are based on the average of 100 measurements performed at the max input voltage for a given range, measured after one year. Calibrator test source high side tied to Channel 0 High, and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute accuracy specifications

Range	Absolute Accuracy
± 10 V	± 2.0 LSB
± 5 V	± 2.0 LSB
± 500 mV	± 3.0 LSB
± 50 mV	± 4.0 LSB

Table 3. Absolute accuracy components - all values are ($\pm$)

Range	% of Reading	Offset (mV)	Averaged Noise + Quantization (mV) ¹	Temp Drift (%/°C)	Absolute Accuracy at FS (mV)
± 10 V	0.0558	2.930	1.262	0.0010	9.77
± 5 V	0.0563	1.460	0.605	0.0010	4.88
± 500 mV	0.1046	0.150	0.057	0.0010	0.73
± 50 mV	0.1340	0.024	0.007	0.0010	0.098

1. Averaged measurements assume dithering and averaging of 100 single-channel readings.

Table 4. Differential non-linearity specifications

All ranges	± 0.5 LSB typ	± 1.0 LSB max
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System throughput

Table 5. System throughput specifications

Condition	Calibration Coefficients	ADC Rate (max)
1. Single channel, single input range.	Per specified range	200 kS/s
2. Multiple channel, single input range	Per specified range	200 kS/s

Condition	Calibration Coefficients	ADC Rate (max)
3. Single channel, multiple input ranges.	Default to value for <code>cbAInScan()</code> range	200 kS/s

Note: For conditions 1-2 above, specified accuracy is maintained at rated throughput. Condition 3 applies a calibration coefficient which corresponds to the range value selected in `cbAInScan()`. This coefficient remains unchanged throughout the scan. Increased settling times may occur during gain-switching operations.

Settling time

Settling time is defined here as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at a specified rate. A -FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6. Settling time specifications

Condition	Range	Accuracy		
		$\pm 0.012\%$ (± 0.5 LSB)	$\pm 0.024\%$ (± 1.0 LSB)	$\pm 0.098\%$ (± 4.0 LSB)
Same range to same range	± 10 V	5 μ S typ	5 μ S max	5 μ S max
	± 5 V	5 μ S typ	5 μ S max	5 μ S max
	± 500 mV	5 μ S typ	5 μ S max	5 μ S max
	± 50 mV	5 μ S typ	5 μ S max	5 μ S max
Any range to any range	-	25 μ S typ	20 μ S typ	15 μ S typ

Parametrics

Table 7. Parametrics specifications

Maximum working voltage (signal + common-mode)	Input must remain within ± 11 V of ground
CMRR @ 60 Hz	± 10 V: 85 dB
	± 5 V: 85 dB
	± 500 mV: 90 dB
	± 50 mV: 90 dB
Small signal bandwidth, all ranges	500 kHz
Large signal bandwidth, all ranges	225 kHz
Input coupling	DC
Input impedance	100 GOhm in normal operation.
	Min 10 MOhm in powered off or overload condition.
Input bias current	± 200 pA

Input offset current	$\pm 100\text{ pA}$
Absolute maximum input voltage	$-40\text{ V to }+55\text{ V}$, power on or off. Protected inputs: ▪ $CH<15:0> IN$ ▪ $AISENSE$
Crosstalk	Adjacent channels: -60 dB
	All other channels: -80 dB

Noise performance

Table 8 summarizes the noise performance for the PCI-DAS6025, PCI-DAS6023. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 8. Analog input noise performance (not including quantization)

Range	Typical Counts Dithered	LSBrms Dithered	Typical Counts Undithered	LSBrms Undithered
$\pm 10\text{ V}$	4	0.6	2	0.1
$\pm 5\text{ V}$	4	0.6	2	0.1
$\pm 500\text{ mV}$	4	0.6	3	0.1
$\pm 50\text{ mV}$	7	0.8	4	0.7

Analog output section (PCI-DAS6025 only)

Table 9. Analog output specifications (PCI-DAS6025)

D/A converter type	Double-buffered, multiplying
Resolution	12-bits, 1-in-4096
Number of channels	2 voltage output
Voltage range	$\pm 10\text{ V}$
Monotonicity	12-bits, guaranteed monotonic
DNL	$\pm 1.0\text{ LSB max}$
Slew rate	$10\text{ V}/\mu\text{s min}$
Settling time	20V step to 0.012% (0.5 LSB): $10\text{ }\mu\text{s max}$
Noise	$200\text{ }\mu\text{Vrms}$, DC to 1 MHz BW
Glitch energy	$\pm 24\text{ mV @ }2\text{ }\mu\text{s duration measured at mid-scale transition.}$
Current drive	$\pm 5\text{ mA}$
Output short-circuit duration	Indefinite @ 25 mA
Output coupling	DC
Output impedance	0.1 ohms max
Power up and reset	DACs cleared to 0 volts $\pm 200\text{ mV max}$

Table 10. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±1.7 LSB

Table 11. Absolute accuracy components

Range	% of Reading	Offset (mV)	Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
±10 V	±0.0219	±5.93	±0.0005	±8.127

Each PCI-DAS6025 is tested at the factory to assure the board's overall error does not exceed ±1.7 LSB.

Table 12. Relative accuracy specifications

Range	Relative Accuracy
±10 V	±0.3 LSB, typical ±0.5 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog output pacing and triggering

Table 13. Analog output pacing and triggering specifications

DAC pacing (SW programmable)	Internal counter – ASIC. Selectable time base: - Internal 40 MHz, 50 ppm stability. - External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate source (SW programmable)	External digital: D/A START TRIGGER
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
DAC trigger sources	External digital: D/A START TRIGGER
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
DAC pacer out	Available at user connector: D/A PACER OUT
RAM buffer size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software selectable.

DMA modes	Demand or non-demand using scatter gather.
Waveform generation throughput	10 kS/s max per channel, 2 channels simultaneous

Analog input/output calibration

Table 14. Analog I/O calibration specifications

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	<i>DC Level: 10.000 V $\pm$ 5 mV. Actual measured values stored in EEPROM.</i>
	Tempco: 5 ppm/ $^{\circ}$ C max, 2 ppm/ $^{\circ}$ C typical
	Long-term stability: 15 ppm, T = 1000 hrs, non-cumulative
Calibration interval	1 year

Digital input/output

Discrete

Table 15. Discrete DIO specifications

Digital type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground (factory configured option).
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, -0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20 V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

82C55 (PCI-DAS6025 only)

Table 16. 82C55 specifications (PCI-DAS6025)

Digital type	82C55
Number of I/O	24 (FIRSTPORTA 0 through FIRSTPORTC 7)
Configuration	2 banks of 8 and 2 banks of 4 or
	3 banks of 8 or
	<i>2 banks of 8 with handshake</i>
Pull up/pull-down configuration	All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground (factory configured option).
<i>Input high voltage</i>	<i>2.0 V min, 5.5 V absolute max</i>
<i>Input low voltage</i>	<i>0.8 V max, -0.5 V absolute min</i>
<i>Output high voltage (IOH = -2.5 mA)</i>	<i>3.0 V min</i>
<i>Output low voltage (IOL = 2.5 mA)</i>	<i>0.4 V max</i>
Power-up / reset state	Input mode (high impedance)

Interrupt section

Table 17. Interrupt specifications

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC Interrupt sources (SW programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.

DAC Interrupt sources (SW programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is 1/4 empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.

Counter section

Table 18. Counter specifications

User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5 V/TTL
CTRn base clock source (software selectable)	Internal 10 MHz, Internal 100 KHz or external connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE).
Counter n output	Available at connector (CTRn OUT).
<i>Clock input frequency</i>	<i>10 MHz max</i>
<i>High pulse width (clock input)</i>	<i>15 ns min</i>
<i>Low pulse width (clock input)</i>	<i>25 ns min</i>
<i>Gate width high</i>	<i>25 ns min</i>
<i>Gate width low</i>	<i>25 ns min</i>
<i>Input low voltage</i>	<i>0.8 V max</i>
<i>Input high voltage</i>	<i>2.0 V min</i>
<i>Output low voltage</i>	<i>0.4 V max</i>
<i>Output high voltage</i>	<i>3.0 V min</i>

Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6025/6023 provides nine user-configurable Trigger/Clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

Table 19. Configurable AUXIN, AUXOUT, and external trigger/clocks

AUXIN<5:0> Sources (SW selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> Sources (SW selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D PACER GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK

Compatibility	5V/TTL
Edge-sensitive polarity	Rising/falling, software selectable
Level-sensitive polarity	Active high/active low, software selectable
Minimum input pulse width	37.5 ns

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 20. DAQ-Sync inter-board triggers/clock specifications

DAQ-Sync signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power consumption

Table 21. Power consumption specifications

+5 V	PCI-DAS6025, PCI-DAS6023: 0.9 A typical, 1.1 A max. Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1 A max, protected with a resettable fuse

Environmental

Table 22. Environmental specifications

Operating temperature range	0 to 55 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 23. Mechanical specifications

Card dimensions	PCI half card: 174.6 mm (L) x 106.9 mm (W) x 11.65 mm (H)
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DAQ-Sync connector and pin out

Table 24. DAQ-Sync connector specifications

Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n: CDS-14-x, 14-pin ribbon cable. x = number of boards

Table 25. DAQ-Sync connector pin out

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

Main connector and pin out

Table 26. Main connector specifications

Connector type	Shielded SCSI 100 D-Type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2 or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P (PCI-DAS6025 only) BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50 SSR-RACK24 (PCI-DAS6025 only, with DADP-5037) CIO-ERB24 (PCI-DAS6025 only, with DADP-5037) CIO-ERB08 (PCI-DAS6025 only, with DADP-5037)
Compatible accessory products (with C100MMS-x cable)	SCB-100

Table 27. 8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0 *
2	CH0 IN HI	52	FIRSTPORTA Bit 1 *
3	CH0 IN LO	53	FIRSTPORTA Bit 2 *
4	CH1 IN HI	54	FIRSTPORTA Bit 3 *
5	CH1 IN LO	55	FIRSTPORTA Bit 4 *
6	CH2 IN HI	56	FIRSTPORTA Bit 5 *
7	CH2 IN LO	57	FIRSTPORTA Bit 6 *
8	CH3 IN HI	58	FIRSTPORTA Bit 7 *
9	CH3 IN LO	59	FIRSTPORTB Bit 0 *
10	CH4 IN HI	60	FIRSTPORTB Bit 1 *
11	CH4 IN LO	61	FIRSTPORTB Bit 2 *
12	CH5 IN HI	62	FIRSTPORTB Bit 3 *
13	CH5 IN LO	63	FIRSTPORTB Bit 4 *
14	CH6 IN HI	64	FIRSTPORTB Bit 5 *
15	CH6 IN LO	65	FIRSTPORTB Bit 6 *
16	CH7 IN HI	66	FIRSTPORTB Bit 7 *
17	CH7 IN LO	67	FIRSTPORTC Bit 0 *
18	LLGND	68	FIRSTPORTC Bit 1 *
19	n/c	69	FIRSTPORTC Bit 2 *
20	n/c	70	FIRSTPORTC Bit 3 *
21	n/c	71	FIRSTPORTC Bit 4 *
22	n/c	72	FIRSTPORTC Bit 5 *
23	n/c	73	FIRSTPORTC Bit 6 *
24	n/c	74	FIRSTPORTC Bit 7 *
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6023

Table 28. 16-channel single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0 *
2	CH0 IN	52	FIRSTPORTA Bit 1 *
3	CH8 IN	53	FIRSTPORTA Bit 2 *
4	CH1 IN	54	FIRSTPORTA Bit 3 *
5	CH9 IN	55	FIRSTPORTA Bit 4 *
6	CH2 IN	56	FIRSTPORTA Bit 5 *
7	CH10 IN	57	FIRSTPORTA Bit 6 *
8	CH3 IN	58	FIRSTPORTA Bit 7 *
9	CH11 IN	59	FIRSTPORTB Bit 0 *
10	CH4 IN	60	FIRSTPORTB Bit 1 *
11	CH12 IN	61	FIRSTPORTB Bit 2 *
12	CH5 IN	62	FIRSTPORTB Bit 3 *
13	CH13 IN	63	FIRSTPORTB Bit 4 *
14	CH6 IN	64	FIRSTPORTB Bit 5 *
15	CH14 IN	65	FIRSTPORTB Bit 6 *
16	CH7 IN	66	FIRSTPORTB Bit 7 *
17	CH15 IN	67	FIRSTPORTC Bit 0 *
18	LLGND	68	FIRSTPORTC Bit 1 *
19	n/c	69	FIRSTPORTC Bit 2 *
20	n/c	70	FIRSTPORTC Bit 3 *
21	n/c	71	FIRSTPORTC Bit 4 *
22	n/c	72	FIRSTPORTC Bit 5 *
23	n/c	73	FIRSTPORTC Bit 6 *
24	n/c	74	FIRSTPORTC Bit 7 *
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6023

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