Specifications

PCI-DAS6034, PCI-DAS6035, and PCI-DAS6036

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog Input Section

A/D converter	Successive Approximation type, min 200kS/s conversion rate.
Resolution	16 bits, 1-in-65536
Number of channels	16 single ended /8 differential, Software selectable
Input ranges	±10V, ±5V, ±500mV, ±50mV, Software selectable
A/D pacing	Internal counter – ASIC. Software selectable time base: ▪ Internal 40MHz, 50ppm stability ▪ External Source via AUXIN<5:0>, Software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 5µS.
A/D Gate Sources	External digital: A/D GATE
A/D gating modes	External digital: Programmable, active high or active low, level or edge
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC Pacer Out	Available at user connector: A/D PACER OUT
RAM buffer size	8K samples
Data transfer	DMA
	Programmed I/O
DMA Modes	Demand or Non-Demand using scatter gather.
Configuration Memory	Up to 8K elements. Programmable channel, gain, and offset
Streaming-to-disk rate	200kS/s, system dependent

Accuracy

200 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1°C of internal calibration temperature and ±10°C of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 1. Absolute Accuracy

Range	Absolute Accuracy
±10V	±10.2 LSB
±5V	±10.9 LSB
±500mV	±19.7 LSB
±50mV	±40.6 LSB

Table 2. Absolute Accuracy Components - All values are (±)

Range	% of Reading	Offset (µV)	Averaged Noise + Quantization (µV)[1]	Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
±10V	0.0239	531	180	0.001	3.10
±5V	0.0262	274	85	0.001	1.67
±500mV	0.0467	54	12.3	0.001	0.30
±50mV	0.0685	21.2	6.54	0.001	0.062

1. Averaged measurements assume averaging of 100 single-channel readings

Each PCI-DAS6036/6035/6034 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in *Table 1* above.

Table 3. Differential non-linearity

All Ranges	±0.5 LSB typ	±1.0 LSB max

System Throughput

Condition	Calibration Coefficients	ADC Rate (max)
Single channel, single input range	Per specified range	200 kS/s
Multiple channel, single input range	Per specified range	200 kS/s
Single channel, multiple input ranges	Default to value for `cbAInScan()` range parameter	200 kS/s

Note: For conditions 1-2 above, specified accuracy is maintained at rated throughput. Condition 3 applies a calibration coefficient which corresponds to the range value selected in cbAInScan (). This coefficient remains unchanged throughout the scan. Increased settling times may occur during gain-switching operations.

Settling Time

Settling time is defined as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Condition	Range	Accuracy	
		±0.0031% (±2.0 LSB)	**±0.0062% (±4.0 LSB)**
Same range to same range	±10V	5µS max	*
	±5V	5µS max	*
	±500mV	5µS typ	*
	±50mV	*	5µS typ

Parametrics

Max working voltage (signal + common-mode)	±11V
CMRR @ 60Hz	±10V Range: 85dB
	±5V Range : 85dB
	±500mV Range: 93dB
	±50mV Range: 93dB
Small signal bandwidth, all ranges	*413 kHz*
Input coupling	*DC*
Input impedance	*100 GOhm in normal operation.*
	2 kOhm typ in powered off or overload condition.
Input bias current	*±200pA*
Input offset current	*±100pA*
Absolute maximum input voltage	*±25V powered on, ±15V powered off.* *Protected Inputs:* ▪ *CH<15:0> IN* ▪ *AISENSE*
Crosstalk	Adjacent Channels: -75dB
	All other Channels: -90dB

Noise Performance

Table 4 below summarizes the noise performance for the PCI-DAS6036/6035/6034. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel-sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 4. Analog Input Noise Performance

Range	Typical Counts	LSBrms
±10V	7	0.7
±5V	7	0.7
±500mV	11	1.1
±50mV	45	5.6

Analog Output Section (PCI-DAS6036 & PCI-DAS6035 only)

	PCI-DAS6035	**PCI-DAS6036**
D/A Converter type	Double-buffered, multiplying	Double-buffered, multiplying
Resolution	12-bits, 1-in-4096	16 bits, 1-in-65536
Number of Channels	2 voltage output	2 voltage output
Voltage Range	±10V	±10V
Monotonicity	*12-bits, guaranteed monotonic*	*16-bits, guaranteed monotonic*
DNL	*±1 LSB max*	*±1 LSB max*
Slew Rate	10V/µs min	15V/µs min
Settling Time (full scale step)	10 µs to ±0.5 LSB accuracy	5 µs to ±1.0 LSB accuracy
Noise	200µVrms, DC to 1MHz BW	110uVrms, DC to 400kHz BW
Glitch Energy	*24mV @ 2µS duration, mid-scale.*	*10mV @ 1µS duration, mid-scale*
Current Drive	±5 mA	±5 mA
Output short-circuit duration	*Indefinite @25mA*	*Indefinite @25mA*
Output coupling	*DC*	*DC*
Output impedance	0.1 ohms max	0.1 ohms max
Power up and reset	DACs cleared to 0 volts ±200mV max	DACs cleared to 0 volts ±21mV max

Table 5. Analog Output Absolute Accuracy

Product	**Range**	**Absolute Accuracy**
PCI-DAS6035	±10V	±1.7 LSB
PCI-DAS6036	±10V	±7.9 LSB

Table 6. Absolute Accuracy Components

Product	**Range**	**% of Reading**	**Offset (mV)**	**Temp Drift (%/DegC)**	**Absolute Accuracy at FS (mV)**
PCI-DAS6035	±10V	±0.022	±5.93	±0.0005	±8.127
PCI-DAS6036	±10V	±0.013	±1.10	±0.0005	±2.417

Each PCI-DAS60356/6035 is tested at the factory to assure the board's overall error does not exceed the absolute accuracy specification listed in *Table 5*.

Table 7. Relative Accuracy

Product	**Range**	**Relative Accuracy**	
PCI-DAS6035	±10V	±0.3 LSB, typical	±0.5 LSB, max
PCI-DAS6036	±10V	-	±2.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog Output Pacing and Triggering

DAC pacing (SW programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40MHz, 50ppm stability. ▪ External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate Source (Software programmable)	External digital: D/A START TRIGGER
	Software gated
DAC gating modes	External digital: ▪ Programmable, active high or active low, level or edge
DAC trigger sources	External digital: D/A START TRIGGER
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
DAC pacer Out	Available at user connector: D/A PACER OUT
RAM Buffer Size	16K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software Selectable.
DMA Modes	Demand or Non-Demand using scatter gather.
Waveform generation Throughput	10 kS/s max per channel, 2 channels simultaneous

Analog Input / Output Calibration

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 10.000V± 5mv. Actual measured values stored in EEPROM.*
	Tempco: 5ppm/°C max, 2ppm/°C typical
	Long-term stability: 15ppm, T = 1000 hrs, non-cumulative
Calibration interval	1 year

Digital Input / Output

Digital Type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5V via 47K resistors (default). Positions available for pull down to ground. Hardware selectable via solder gap.
Input high voltage	2.0V min, 7.0V absolute max
Input low voltage	0.8V max, –0.5V absolute min
Output high voltage (IOH = -32mA)	3.80V min, 4.20V typ
Output low voltage (IOL = 32mA)	0.55V max, 0.22V typ
Data Transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupt Section

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC Interrupt sources (Software Programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (Software Programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.

Counter Section

User counter type	82C54
Number of Channels	2
Resolution	16-bits
Compatibility	5V/TTL
CTRn base clock source (Software selectable)	Internal 10MHz, Internal 100KHz or External connector (CTRn CLK)
Internal 10MHz clock source stability	50ppm
Counter n Gate	Available at connector (CTRn GATE).
Counter n Output	Available at connector (CTRn OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15ns min*
Low pulse width (clock input)	*25ns min*
Gate width high	*25ns min*
Gate width low	*25ns min*
Input low voltage	*0.8V max*
Input high voltage	*2.0V min*
Output low voltage	*0.4V max*
Output high voltage	*3.0V min*

Configurable AUXIN<5:0>, AUXOUT<2:0> External Trigger/Clocks

The PCI-DAS6036/6035/6034 provides nine user-configurable Trigger/Clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

AUXIN<5:0> Sources (SW selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer timebase
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer timebase
AUXOUT<2:0> Sources (SW selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK	CTR1 clock source
	D/A UPDATE	D/A update pulse
	CTR2 CLK	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	D/A START TRIGGER:	DAC Start Trigger Out
Default Selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D PACER GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5V/TTL	
Edge-sensitive polarity	Rising/falling, software selectable	
Level-sensitive polarity	Active high/active low, software selectable	
Minimum input pulse width	37.5ns	

DAQ-Sync inter-board Triggers/Clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

DAQ-Sync Signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power Consumption

+5V	0.9A typical, 1.1A max. Does not include power consumed through the I/O connector.
+5V available at I/O connector	1A max, protected with a resettable fuse

Environmental

Operating Temperature Range	0 to 55°C
Storage Temperature Range	-20 to 70°C
Humidity	0 to 90% non-condensing

Mechanical

Card dimensions	PCI half card: 174.4mm(L) x 100.6mm(W) x11.65mm(H)

DAQ-Sync Connector and Pin Out

Connector type	14-Pin right-angle 100mil box header
Compatible Cable	MCC p/n: CDS-14-x, 14 pin ribbon cable. x = number of boards (2 - 5)

Pin	**Signal Name**
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

Main Connector and Pin Out

Connector type	Shielded SCSI 100 D-Type
Compatible Cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2 or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P (PCI-DAS6036/6035 only) BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100

8 Channel Differential Mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN HI	52	n/c
3	CH0 IN LO	53	n/c
4	CH1 IN HI	54	n/c
5	CH1 IN LO	55	n/c
6	CH2 IN HI	56	n/c
7	CH2 IN LO	57	n/c
8	CH3 IN HI	58	n/c
9	CH3 IN LO	59	n/c
10	CH4 IN HI	60	n/c
11	CH4 IN LO	61	n/c
12	CH5 IN HI	62	n/c
13	CH5 IN LO	63	n/c
14	CH6 IN HI	64	n/c
15	CH6 IN LO	65	n/c
16	CH7 IN HI	66	n/c
17	CH7 IN LO	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = n/c on PCI-DAS6034

16 Channel Single-Ended Mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN	52	n/c
3	CH8 IN	53	n/c
4	CH1 IN	54	n/c
5	CH9 IN	55	n/c
6	CH2 IN	56	n/c
7	CH10 IN	57	n/c
8	CH3 IN	58	n/c
9	CH11 IN	59	n/c
10	CH4 IN	60	n/c
11	CH12 IN	61	n/c
12	CH5 IN	62	n/c
13	CH13 IN	63	n/c
14	CH6 IN	64	n/c
15	CH14 IN	65	n/c
16	CH7 IN	66	n/c
17	CH15 IN	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND*	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = n/c on PCI-DAS6034

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