Specifications

PCI-DAS6030 & PCI-DAS6032

Document Revision 1.2, November, 2003

Specifications

Typical for 25°C unless otherwise specified.

Analog Input

Table 1 - Analog Input Specifications

A/D converter	Successive Approximation type
Resolution	16 bits, 1 in 65536
Maximum Sample Rate	100 kS/s
Number of channels	16 single ended / 8 differential, software selectable
Input ranges	Bipolar: ±10V, ±5V, ±2V, ±1V, ±0.5V, ±0.2V, ±0.1V Unipolar: 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V, 0 to 0.1V Software selectable
A/D pacing	Internal counter – ASIC. Software selectable time base: ▪ Internal 40MHz, 50ppm stability ▪ External Source via AUXIN<5:0>, Software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 10μS.
A/D Gate Sources	External digital: A/D GATE
	External analog: ATRIG input CH0 IN through CH15 IN
A/D gating modes	External digital: Programmable, active high or active low, level or edge.
	External analog: See Analog Trigger section (page 8)
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: See Analog Trigger section (page 8)
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC Pacer Out	Available at user connector: A/D PACER OUT
RAM buffer size	8K samples
Data transfer	DMA
	Programmed I/O
DMA Modes	Demand or Non-Demand using scatter-gather.
Configuration Memory	Up to 8K elements. Programmable channel, gain, and offset.
Streaming-to-disk rate	100 kS/s, system dependent

Accuracy

100 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1°C of internal calibration temperature and ±10°C of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2 - Absolute Accuracy

Range	Absolute Accuracy
±10V	±3.81 LSB
±5V	±13.61 LSB
±2 V	±13.69 LSB
±1V	±13.83 LSB
±500mV	±14.09 LSB
±200mV	±16.71 LSB
±100mV	±19.99 LSB
0 to 10V	±6.40 LSB
0 to 5V	±26.11 LSB
0 to 2V	±26.28 LSB
0 to 1V	±26.54 LSB
0 to 500mV	±27.13 LSB
0 to 200mV	±32.11 LSB
0 to 100mV	±38.70 LSB

Table 3 - Absolute Accuracy Components – All values are (±)

Range	% of Reading	Offset (µV)	Noise +Quantization (µV)		Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged[1]		
±10V	0.0061	479.2	634.1	54.9	0.0001	1.147
±5V	0.0361	243.6	317.1	27.5	0.0006	2.077
±2V	0.0361	102.2	126.8	11.0	0.0006	0.836
±1V	0.0361	55.1	63.4	5.5	0.0006	0.422
±500mV	0.0361	31.6	36.8	3.2	0.0006	0.215
±200mV	0.0411	17.4	22.5	2.0	0.0006	0.102
±100mV	0.0461	12.7	19.6	1.8	0.0006	0.061
0 to 10V	0.0061	326.6	417.8	36.6	0.0001	0.976
0 to 5V	0.0361	167.3	208.9	18.3	0.0006	1.992
0 to 2V	0.0361	71.7	83.6	7.3	0.0006	0.802
0 to 1V	0.0361	39.9	41.8	3.7	0.0006	0.405
0 to 500mV	0.0361	23.9	28.1	2.5	0.0006	0.207
0 to 200mV	0.0411	14.4	19.6	1.8	0.0006	0.098
0 to 100mV	0.0461	11.2	18.1	1.7	0.0006	0.059

1. Averaged measurements assume averaging of 100 single-channel readings.

Each PCI-DAS6030 and PCI-DAS6032 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in *Table 2*.

Table 4 - Relative Accuracy – All values are (±)

Range	**Relative Accuracy (µV)**	
	Single Point	**Averaged [1]**
±10V	723.3	72.3
±5V	361.6	36.2
±2V	144.7	14.5
±1V	72.3	7.2
±500mV	42.2	4.2
±200mV	26.5	2.7
±100mV	24.1	2.4
0 to 10V	482.2	48.2
0 to 5V	241.1	24.1
0 to 2V	96.4	9.6
0 to 1V	48.2	4.8
0 to 500mV	33.1	3.3
0 to 200mV	24.1	2.4
0 to 100mV	22.9	2.3

1. Averaged measurements assume averaging of 100 single-channel readings

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 5 - Differential non-linearity

All Ranges	±0.5 LSB typ	±1.0 LSB max

Settling Time

Settling time is defined as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6 - Settling Time

Condition	Range	±0.00076% (±0.5 LSB)	±0.0015% (±1 LSB)	±0.0061% (±4 LSB)	±0.012% (±8 LSB)
Same range to same range	±10V	40µS max	20µS max	10µS max	5µS typ
	±5V	40µS max	20µS max	10µS max	5µS typ
	±2V	40µS max	20µS max	10µS max	5µS typ
	±1V	40µS max	20µS max	10µS max	5µS typ
	±500mV	40µS max	20µS max	10µS max	5µS typ
	±200mV	40µS max	20µS max	10µS max	5µS typ
	±100mV	40µS max	20µS max	10µS max	5µS typ
	0 to 10V	40µS max	20µS max	10µS max	5µS typ
	0 to 5V	40µS max	20µS max	10µS max	5µS typ
	0 to 2V	40µS max	20µS max	10µS max	5µS typ
	0 to 1V	40µS max	20µS max	10µS max	5µS typ
	0 to 500mV	40µS max	20µS max	10µS max	5µS typ
	0 to 200mV	40µS max	20µS max	10µS max	5µS typ
	0 to 100mV	40µS max	20µS max	10µS max	5µS typ

Parametrics

Table 7 - Parametrics

Max working voltage (signal + common-mode)	±11V
CMRR @ 60Hz	±10V Range & 0 to 10V: 92dB
	±5V Range & 0 to 5V: 97dB
	±2V Range & 0 to 2V: 101dB
	±1V Range & 0 to 1V: 104dB
	±0.5V Range & 0 to 0.5V: 105dB
	±0.2V Range & 0 to 0.2V: 105dB
	±0.1V Range & 0 to 0.1V: 105dB
Small signal bandwidth, all ranges	255 kHz
Input coupling	DC
Input impedance	100 GOhm in normal operation. 820 Ohm typ in powered off or overload condition.
Input bias current	±200pA
Input offset current	±100pA

Absolute maximum input voltage	±25V power on, ±15V power off. Protected Inputs: ▪ CH<15:0> IN ▪ AISENSE
Crosstalk	Adjacent channels: -75dB
	All other channels: -90dB

Noise Performance

Table 8 below summarizes the noise performance for the PCI-DAS6030 and PCI-DAS6032. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector. Samples are gathered 100kS/s sampling rate. The specification applies to both single-ended and differential modes of operation.

Table 8 – Analog Input Noise Performance

Range	LSBrms	Typical Counts
±10V	0.6	8
±5V	0.6	8
±2V	0.6	8
±1V	0.6	8
±500mV	0.7	8
±200mV	1.1	11
±100mV	2.0	17
0 to 10V	0.8	8
0 to 5V	0.8	8
0 to 2V	0.8	8
0 to 1V	0.8	8
0 to 500mV	1.1	11
0 to 200mV	2.0	17
0 to 100mV	3.8	25

Analog Output Section (PCI-DAS6030 only)

Table 9 – PCI-DAS6030 Analog Output Specifications

D/A Converter type	Double-buffered, multiplying
Resolution	16-bits, 1 in 65536
Number of Channels	2 voltage output
Voltage Range	±10V, 0 to 10V, software selectable
Monotonicity	16-bits, guaranteed
Update Range	100 kS/s per channel
Slew Rate	5V/µs typ.
Settling Time (full scale step)	10µs max to ±1LSB
Noise	60µVrms, DC to 1MHz BW
Current Drive	±5 mA
Output short-circuit duration	Indefinite @25mA
Output coupling	DC
Output impedance	0.1 Ohms max.
Power up and reset	DACs cleared to 0 volts ±20mV max.

Table 10 – Analog Output Absolute Accuracy

Range	**Absolute Accuracy**
±10V	±4.7 LSB
0 to 10V	±7.9 LSB

Table 11 – Absolute Accuracy Components - All values are (±)

Range	**% of Reading**	**Offset (µV)**	**Temp Drift (%/ºC)**	**Absolute Accuracy at FS (mV)**
±10V	0.0062	813	0.0001	1.430
0 to 10V	0.0062	584	0.0001	1.201

Each PCI-DAS6030 is tested at the factory to assure that the board's overall error does not exceed the values specified in *Table 10*.

Table 12 – Relative Accuracy

Range	**Relative Accuracy**	
All Ranges	±0.5 LSB, typical	±1.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog Output Pacing and Triggering

Table 13 – Analog Output Pacing and Triggering

DAC pacing (Software programmable)	Internal counter – ASIC. Selectable time base: Internal 40MHz, 50ppm stability. External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate Sources (Software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software gated
DAC gating modes	External digital: ▪ Programmable, active high or active low, level or edge
	External analog: See Analog Trigger section
DAC trigger sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for Positive or Negative slope.
DAC pacer Out	Available at user connector D/A PACER OUT
RAM Buffer Size	16K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software selectable.
DMA Modes	Demand or Non-Demand using scatter gather.
Waveform generation Throughput	100 kS/s max per channel, 2 channels simultaneous

Analog Trigger

Table 14 – Analog Trigger

Analog Trigger Sources Software selectable	External: ATRIG input CH0 IN through CH15 IN, first channel in scan	
Analog Trigger Levels	ATRIG input: ±10V	
	CH0 IN through CH15 IN: ± Full-scale, range dependent	
Analog Trigger Modes	External analog: Software-configurable for: ▪ Positive or Negative slope	
Analog Gate Modes	External analog: Software-configurable for: ▪ Above or Below reference ▪ Positive or Negative hysteresis ▪ In or Out of window	
Resolution	12-bits, 1-in-4096	
Accuracy	±1% Full-scale range max	
Bandwidth (-3dB)	ATRIG input	4 MHz
	CH0 IN through CH15 IN	255 kHz

Analog Input / Output Calibration

Table 15 – Analog I/O Calibration

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	DC Level: 5.000V± 1mV. Actual measured values stored in EEPROM.
	Tempco: 0.6ppm/°C max
	Long-term stability: ±6ppm/sqrt(1000 hrs)
Calibration interval	1 year

Digital Input / Output

Table 16 – Digital I/O

Digital Type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5V via 47K resistors (default). Positions available for pull down to ground. Hardware selectable via solder gap.
Input high voltage	2.0V min, 7.0V absolute max
Input low voltage	0.8V max, –0.5V absolute min
Output high voltage (IOH = -32mA)	3.80V min, 4.20V typ
Output low voltage (IOL = 32mA)	0.55V max, 0.22V typ
Data Transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupt Section

Table 17 – Interrupts

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC Interrupt sources (Software Programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (Software Programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.

Counter Section

Table 18 – Counters

User counter type	82C54
Number of Channels	2
Resolution	16-bits
Compatibility	5V/TTL
CTRn base clock source (Software selectable)	Internal 10MHz, Internal 100kHz or External connector (CTRn CLK)
Internal 10MHz clock source stability	50ppm
Counter n Gate	Available at connector (CTRn GATE).
Counter n Output	Available at connector (CTRn OUT).
Clock input frequency	10 MHz max
High pulse width (clock input)	15ns min
Low pulse width (clock input)	25ns min
Gate width high	25ns min
Gate width low	25ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Configurable AUXIN<5:0>, AUXOUT<2:0> External Trigger/Clocks

The PCI-DAS6030 and PCI-DAS6032 provide nine user-configurable Trigger/Clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

Table 19 – Configurable Triggers/Clocks

AUXIN<5:0> Sources (SW selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> Sources (SW selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC Start Trigger Out
Default Selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5V/TTL	
Minimum pulse width	37.5ns	

DAQ-Sync inter-board Triggers/Clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 20 – DAQ-Sync Signals

DAQ-Sync Signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power Consumption

Table 21 – Power Consumption Specifications

+5V	PCI-DAS6030/32: 1.3A typical, 1.5A max. Does not include power consumed through the I/O connector.
+5V available at I/O connector	1A max, protected with a resettable fuse

Environmental

Table 22 – Environmental Specifications

Operating Temperature Range	0 to 55°C
Storage Temperature Range	-20 to 70°C
Humidity	0 to 90% non-condensing

Mechanical

Table 23 – Mechanical Specifications

Card dimensions	PCI half card: 174.4mm(L) x 106.9mm(W) x11.65mm(H)

DAQ-Sync Connector and Pin-Out

Table 24 – DAQ-Sync Connector Specifications

Connector type	14-pin right-angle 100mil box header
Compatible Cables	MCC p/n: CDS-14-x, 14 pin ribbon cable. x = number of boards

Table 25 – DAQ-Sync Connector Pin-out

Pin	**Signal Name**
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

Main Connector and Pin-Out

Table 26 – Main Connector Specifications

Connector type	Shielded SCSI 100 D-Type
Compatible Cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100

Table 27 – 8 Channel Differential Mode Pin-out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN HI	52	n/c
3	CH0 IN LO	53	n/c
4	CH1 IN HI	54	n/c
5	CH1 IN LO	55	n/c
6	CH2 IN HI	56	n/c
7	CH2 IN LO	57	n/c
8	CH3 IN HI	58	n/c
9	CH3 IN LO	59	n/c
10	CH4 IN HI	60	n/c
11	CH4 IN LO	61	n/c
12	CH5 IN HI	62	n/c
13	CH5 IN LO	63	n/c
14	CH6 IN HI	64	n/c
15	CH6 IN LO	65	n/c
16	CH7 IN HI	66	n/c
17	CH7 IN LO	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT0*	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6032

Table 28 – 16 Channel Single-Ended Mode Pin-out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN	52	n/c
3	CH8 IN	53	n/c
4	CH1 IN	54	n/c
5	CH9 IN	55	n/c
6	CH2 IN	56	n/c
7	CH10 IN	57	n/c
8	CH3 IN	58	n/c
9	CH11 IN	59	n/c
10	CH4 IN	60	n/c
11	CH12 IN	61	n/c
12	CH5 IN	62	n/c
13	CH13 IN	63	n/c
14	CH6 IN	64	n/c
15	CH14 IN	65	n/c
16	CH7 IN	66	n/c
17	CH15 IN	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT0*	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6032

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