# PCI-DDA02/16, PCI-DDA04/16, PCI-DDA08/16 Analog Output Board User's Guide



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# 1 INTRODUCTION

Thank you for purchasing a top quality PC data acquisition and control board from Measurement Computing Corporation. The PCI-DDA0#/16 family of boards represent the latest technology from Measurement Computing. As there are no switches or jumpers on the board, you will find the PCI-DDA0#/16 board very easy to install and use.

All configuration, calibration, and range settings are done solely through software, making installation simple and quick. The PCI-DDA0#/16 family is supported by Measurement Computing Corporation's innovative Universal Library and DAS-Wizard software, as well as by most third-party, high-level data acquisition software such as SoftWIRE. Thus, you have all the tools you need to accomplish your data acquisition task.

Go ahead and install the PCI-DDA0#/16 into your computer and then turn your computer on.

PLEASE NOTE: If you have a PCI-DDA08/16, all instructions in this manual apply. If you have a PCI-DDA04/16, you should ignore all references to D/A channels 4 through 7; and if you have a PCI-DDA02/16, you should ignore all references to D/A channels 2 through 7. In all other respects, the three models are identical.

# 2 PRODUCT DESCRIPTION

The PCI-DDA0#/16 family comprises three PCI bus plug-in board models: PCI-DDA02/16 (Figure 2-1), PCI-DDA04/16 (Figure 2-2), and PCI-DDA08/16 (Figure 2-3). These boards have two, four, or eight, 16-bit analog output channels, respectively. In addition, each model has 48 digital I/O lines.

The D/A converters can be independently configured for either bipolar or unipolar 2.5V, 5V, and 10V ranges. The outputs may be updated individually or simultaneously. All calibration and range settings are done through software.

The digital I/O ports are configured as two 8255 mode 0 emulations, each consisting of four ports: Port A (8 bits), Port B (8 bits), Port C high (4 bits), and Port C low (4 bits). The digital outputs are capable of sinking 64 mA and sourcing 15 mA utilizing standard "S" logic.

The PCI interface uses the PLX 9052 IC which is a slave-only device. The PCI interface for the analog output is configured in a 16 bit, multiplexed address/data bus, I/O access mode. The PCI interface for the digital I/O is configured in an 8 bit, multiplexed address/data bus, I/O access mode to be register compatible with the PCI-DIO##H and PCI-DIO48/CTR15 boards. For an idea of how the PCI-DDA0#/16 is logically constructed, refer to the block diagram below according to your particular model.

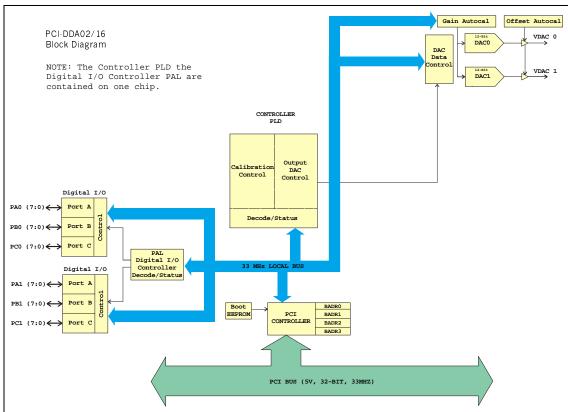


Figure 2-1. PCI-DDA02/16 Block Diagram

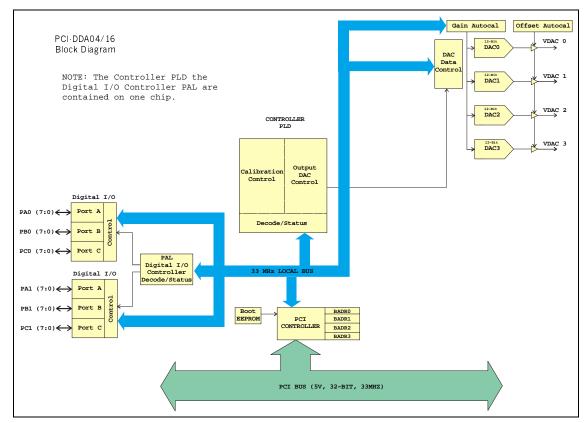


Figure 2-3. PCI-DDA04/16 Block Diagram

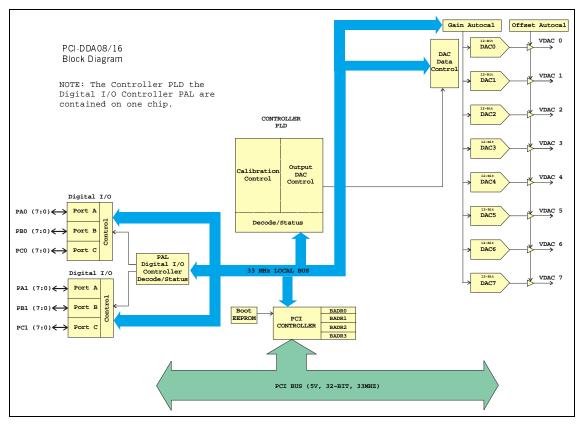


Figure 2-3. PCI-DDA08/16 Block Diagram

The PCI-DDA0#/16 is completely plug and play. There are no switches or jumpers to set. Configuration is controlled by your systems' BIOS. Simply turn off your PC, open it up and insert the PCI-DDA0#/16 into any available PCI slot.

If you are using an operating system with support for Plug and Play (such as Windows 95 or 98), a dialog box will pop up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for a disk containing it. The InstaCal software that was supplied with your board contains this file. Just insert the disk or CD and click OK.

In order to easily test your installation, it is recommended that you install InstaCal, the installation, calibration and test utility that was supplied with your board. Refer to the *Software Installation Manual* for information on the initial setup, loading, and installation of InstaCal and the optional Universal Library software.

# 4 CONNECTIONS

The PCI-DDA0#/16 uses a single 100-pin high density connector on the back plate of the board to bring out all required digital and analog lines and grounds.

NOTE: If you have a PCI-DDA08/16, all instructions in this manual apply. If you have a PCI-DDA04/16, ignore all references to D/A channels 4 through 7; and if you have a PCI-DDA02/16, ignore all references to D/A channels 2 through 7. In all other respects, the three models are identical.

#### 4.1 CONNECTING EXTERNAL LINES

The 100-pin, high density connector provides a far greater signal density than the traditional 37 pin D type connector. The ideal means for breaking out the 100 lines from the PCI-DDA0#/16 are a combination of a C100HDS-6 six foot shielded cable or a C100HDS-3 three foot shielded cable and the SCB-100 breakout box, both available from Measurement Computing.

Alternatively, a C100HD50-6 six foot ribbon cable or a C100HD50-3 three foot ribbon cable could be used with one SCB-50, one CIO-TERM100 or two CIO-MINI50's.

#### 4.2 ANALOG CONNECTIONS

The analog output connections on the PCI-DDA0#/16 series are two-wire hookups, one end of which is the signal labeled Vout#, with # being the channel number from 0 to 7 (PCI-DDA08/16), 0 to 3 (PCI-DDA04/16), or 0 to 1 (PCI-DDA02/16). The other end is the associated analog ground. In software, you may select analog ranges of  $\pm 10$ V,  $\pm 5$ V,  $\pm 2.5$ V, 0 to 10V, 0 to 5V, and 0 to 2.5V. Each port may be reconfigured easily and quickly.

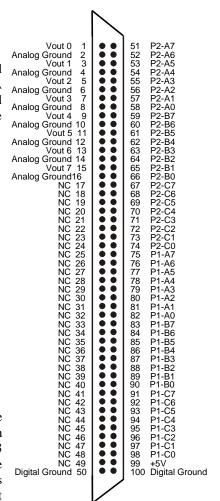


Figure 4-1. 100-Pin, High-Density Connector

### 4.3 DIGITAL CONNECTIONS

The PCI-DDA0#/16 emulates two 82C55 chips, but offers much higher drive capability than the 82C55. The board emulates only Mode 0 of the 82C55 (no strobed I/O or bi-directional I/O bits). The board is completely plug-and-play without any onboard user configurable switches or jumpers. The 48 CMOS/TTL compatible digital I/O lines are configured in four banks of eight and four banks of four. Each bank may be input or output.

All the digital outputs/inputs on the PCI-DDA0#/16 connector are TTL-compatible. TTL is an electronics industry term, short for Transistor Transistor Logic, a standard for digital signals which are either at near 0V or near 5V. The outputs are capable of sinking 64 mA or sourcing 15 mA. All I/O is brought out to the 100-pin connector, which also allows connection to the PC's +5 Volt and Ground.

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines. In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0. In the absence of a pull-up/down resistor, any digital input which is unconnected is unspecified.

You do not have to connect all input lines; unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

### 4.4 PULL UP AND PULL DOWN RESISTORS

#### NOTE: Whenever the board is powered-on or reset, all ports are set to input mode.

Inputs will typically float high, but will not reliably supply enough output current to ensure that external devices you have connected will "see" a logic 1. Which way they float depends on the characteristics of the circuits connected and is unpredictable! If it is important that your system go into a predetermined state on power up or reset, you need pull up/pull down resistors. (Order 2.2K 9PU.)

The pull-up resistor pulls the input to a high state (+5V). Its resistance of 2200 ohms draws only 2 ma of the 64 mA available from the output. A 2200 ohm pull-down resistor does the same task except that the line is pulled low when the board is in the input mode (and uses only 2 mA of the 15 mA available output provided by the board). The PCI-DDA0# board has positions for up to six Single Inline Package (SIPs) resistors. The positions are marked Port 0 A, B and C, and Port 1 A, B and C. The positions are located directly adjacent to the board's I/O connector. The SIP resistors will provide either pull-up or pull-down action for each eight-line port depending on their orientation in the port positions on the board.

In a nine-pin SIP resistor, one end of all eight 2.2 kOhm resistors are connected to a single (common) pin. The common pin, marked with a dot, is at one end of the SIP. The other eight pins are connect to each resistor.

When oriented as required and soldered in the board, all eight SIP resistor pins are either pull-up or pull-down.

At each SIP position on the board there are ten holes in a line. The hole on one end of the line is marked "HI" (+5V); the hole on the other end is marked "LO" (GND). The holes in between connect to the eight lines of a port.

For pull-up (per port), insert a SIP with the common pin (dotted) in the HI hole. For pull-down (per port), insert a SIP with the common pin in the LO hole.

If required, individual 2.2 kOhm resistors can be substituted for the resistor SIPs.

# 5 PROGRAMMING & APPLICATIONS

Your PCI-DDA0#/16 is supported by Measurement Computing Corporation's powerful Universal Library. We strongly recommend that you take advantage of the Universal Library as your software interface. The complexity of the registers required for automatic calibration combined with the dynamic allocation of addresses and internal resources makes the PCI-DDA0#/16 series very challenging to program via direct register I/O operations. Direct I/O programming should not be required.

# 5.1 PROGRAMMING LANGUAGES

Measurement Computing Corporation's Universal Library provides complete access to the PCI-DDA0#/16 functions from a range of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic or any other language, please refer to the Universal Library manual.

### 5.2 PACKAGED THIRD-PARTY APPLICATIONS PROGRAMS

In addition to Measurement Computing Corporation's DAS-Wizard, many packaged third-party application programs such as SoftWIRE and HP-VEE now have drivers for the PCI-DDA0#/16. If your package does not appear to have drivers for the PCI-DDA0#/16, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise you on how to obtain PCI-DDA0#/16 drivers.

Some application drivers that are included with Universal Library are not included with third-party application packages. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us for more information on this topic.

The PCI-DDA0#/16 is shipped fully-calibrated from the factory with calibration coefficients stored in nonvolatile RAM. When using the Universal Library, these calibration factors are read from nonvolatile RAM and are automatically written to the calibration DACS each time a different DAC range is specified. The user has the option to recalibrate with respect to the factory-measured voltage standards at any time by simply selecting the "Calibrate" option in InstaCal. InstaCal will calibrate all channels at all six ranges. Each channel takes less than a minute to calibrate.

### 6.1 CALIBRATION CONFIGURATION

The PCI-DDA0#/16 provides self-calibration of the analog source and measure systems thereby eliminating the need for external equipment and user adjustments. The analog output circuits are calibrated for both gain and offset. Gain calibration of the analog outputs are performed via DAC reference adjustments. Offset adjustments for the analog output are made in the output buffer section. A block diagram of the PCI-DDA0#/16 series calibration circuitry is shown in Figure 6-1 below.

# Gain Adjust 16-bit Output DAC PGA Serial MAX542 Output Voltage Trim DACs Fine Offset Adjust Coarse Precision 2.5V Output Trim DACs 8x1 **Voltages** Programable Voltage source COMP Precision MAX515 Counter Comparator Fine serial MAX542 Setpoint Voltage Reference DAC CLEAR

## PCI-DDA0x/16 Calibration Block Diagram

Figure 6-1. PCI-DDA0#/16 Calibration Block Diagram

# 6.2 "IN-SYSTEM" CALIBRATION

The PCI-DDA0#/16 is calibrated at the factory for the correct voltages at the I/O connector itself. For more precise application of voltages at the "system end", we can provide a version of InstaCAL that allows you to calibrate the board within your system, for correct voltages at your field connection. This calibration allows the user to remove the effects of voltage drops caused by IR loss in the cable and connector for resistances up to 1 ohm. This calibration will also allow the user to zero out errors in any external signal conditioning up to approximately  $\pm 10$  mV.

In most applications, the version of InstaCal that ships with the board will provide the accuracy specified. If you have an application with unusual requirements (long cables, etc.), you may need the "in-system version" to achieve this accuracy. In this case, please contact the factory for details regarding the use of this "in-system" calibration feature.

We strongly urge users to take advantage of the Universal Library software package rather than attempt to write register level software for the PCI-DDA0#/16 series. The register level programming information provided here is intended to be for information only. Register level programming of this or any other software calibrating PCI board is quite complex and should only be attempted by experienced programmers.

### 7.1 REGISTER OVERVIEW

NOTE: Ignore references to D/A channels 4 through 7 on the PCI-DDA04/16, and references to channels 2 through 7 on the PCI-DDA02/16. Otherwise, the three boards are identical.

PCI-DDA0#/16 operation registers are mapped into I/O space. Unlike ISA bus designs, this board has several base addresses, each corresponding to a reserved block of addresses in I/O space.

Of the six Base Address Regions (BADR) available per the PCI 2.1 specification, four are implemented in this design and are summarized as follows.

I/O Region	Function	Operations		
BADR0	PCI memory mapped configuration registers	32-bit DOUBLE WORD		
BADR1	PCI I/O mapped configuration registers	32-bit DOUBLE WORD		
BADR2	Digital I/O registers	8-bit BYTE		
BADR3	DAC registers	16-bit WORD		

Table 7-1. BADR Register Summary

BADR0 and BADR1 are used for PCI configuration and have no user functions.

BADR2 is an 8-bit data/address bus for compatibility with our other digital I/O PCI cards. BADR3 is a 16-bit data/address bus.

# **7.2** BADR2

Table 7-2. BADR2 Read/Write Functions

Register	Read Function	Write Function
BADR2 + 0	Input Port 1A Data	Output Port 1A Data
BADR2 + 1	Input Port 1B Data	Output Port 1B Data
BADR2 + 2	Input Port 1C Data	Output Port 1C Data
BADR2 + 3	Control register readback 1	Control Register 1
BADR2 + 4	Input Port 2A Data	Output Port 2A Data
BADR2 + 5	Input Port 2B Data	Output Port 2B Data
BADR2 + 6	Input Port 2C Data	Output Port 2C Data
BADR2 + 7	Control register readback 2	Control Register 2

The Digital I/O ports simulate the 8255 Mode 0 function.

#### **PORT 1A DATA**

BADR2 + 0h

#### READ/WRITE

7	6	5	4	3	2	1	0		
A7	A6	A5	A4	A3	A2	A1	A0		

#### **PORT 1B DATA**

BADR2 + 1h

### READ/WRITE

7	6	5	4	3	2	1	0
В7	В6	B5	B4	В3	B2	B1	В0

### **PORT 1C DATA**

BADR2 + 02h

#### READ/WRITE

- 3								
	7	6	5	4	3	2	1	0
	СНЗ	CH2	CH1	CH0	CL3	CL2	CL1	CL0

# **CONTROL REGISTER 1**

BADR2 + 03h

# READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

The operating mode of the Digital I/O port is set to Mode 0. The control register therefore is used to enable the ports for input/output to the connector. For example, to set all ports to output, write the value 0h to BADR2 + 3. To set all ports to input, write the value 1Bh to BADR2 + 3. The user is able to read the current state of the output port by simply reading that port when configured for output. Codes D7, D6, D5, and D2 are 'don't care'. 'CU' is PORT C upper nibble, 'CL' is PORT C lower nibble.

Table 7-3. BADR2 Code Functions

Progra	mming (	Codes		Values		DIO Por	rt		
<u>D4</u>	<u>D3</u>	<u>D1</u>	<u>D0</u>	<u>H</u>	<u>Dec</u>	<u>A</u>	<u>B</u>	<u>CU</u>	<u>CL</u>
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	IN	OUT	OUT
0	0	1	1	3	3	OUT	IN	OUT	IN
0	1	0	0	8	8	OUT	OUT	IN	OUT
0	1	0	1	9	9	OUT	OUT	IN	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	В	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	IN	OUT	OUT
1	0	1	1	13	19	IN	IN	OUT	IN
1	1	0	0	18	24	IN	OUT	IN	OUT
1	1	0	1	19	25	IN	OUT	IN	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

### **PORT 2A DATA**

BADR2 + 04h

# READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#### **PORT 2B DATA**

BADR2 + 05h

### READ/WRITE

7	6	5	4	3	2	1	0
В7	B6	B5	B4	В3	B2	B1	В0

# **PORT 2C DATA**

BADR2 + 06h

# READ/WRITE

7	6	5	4	3	2	1	0
СНЗ	CH2	CH1	CH0	CL3	CL2	CL1	CL0

### **CONTROL REGISTER 2**

BADR2 + 07h

### READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

See BADR2  $\pm$  03h and TABLE 1.0 for full description of the Control Register.

# **7.3** BADR3

Table 7-4. BADR3 Read/Write Functions

REGISTER	READ FUNCTION	WRITE FUNCTION
BADR3 + 0	Initiate a simultaneous update	D/A Control Register
BADR3 + 2h		reserved
BADR3 + 4h	D/A Calibration Register 1 Data	D/A Calibration Register 1
BADR3 + 6h		D/A Calibration Register 2
BADR3 + 8h		D/A 0 DATA
BADR3 + Ah		D/A 1 DATA
BADR3 + Ch		D/A 2 DATA
BADR3 + Eh		D/A 3 DATA
BADR3 + 10h		D/A 4 DATA
BADR3 + 12h		D/A 5 DATA
BADR3 + 14h		D/A 6 DATA
BADR3 + 16h		D/A 7 DATA

#### D/A CONTROL REGISTER

BADR3 + 0h

#### READ/WRITE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	R2	R1	R0	X	D2	D1	D0	EN	SU

#### WRITE

SU

This bit enables simultaneous update for the DAC specified by D2, D1, and D0 (see table below). Setting the simultaneous update bit inhibits updating the DAC output until a simultaneous update is initiated (see READ below).

0 = Simultaneous update disabled

1 = Simultaneous update enabled

The power-on status of this bit is 0

**NOTE:** Writing to any DAC that does not have its SU bit set will also initiate an update. Therefore, load all the DACs with the SU bit set and then initiate the update before writing to any other DAC.

**EN** This bit enables the DAC specified by D2, D1, D0.

0 = DAC disabled

1 = DAC enabled

The power-on status of this bit is 0. A disabled DAC is pulled to 0v.

**D[2:0]** These bits specify the DAC that is being configured.

Figure 7-5. DAC Channel Coding

D2	D1	<b>D</b> 0	DAC Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

**R[2:0]** These bits select the gain/range for the DAC specified by D2, D1, and D0. The DACs power up at 0V (-FS) in the unipolar 10V range.

Figure 7-6. BADR3 Unipolar/Bipolar Gain/Range Coding

R2	R1	R0	RANGE	LSB Size
0	0	X	Bipolar 2.5V	76.3µV
0	1	0	Bipolar 5V	152.6μV
0	1	1	Bipolar 10V	305.2μV
1	0	X	Unipolar 2.5V	38.1µV
1	1	0	Unipolar 5V	76.3µV
1	1	1	Unipolar 10V	152.6μV

#### READ

Reading this register initiates a simultaneous update for all DACs.

#### D/A CALIBRATION REGISTER 1

BADR3 + 4h

Use InstaCal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond he scope of this document. If you need to program the calibration registers, please contact the factory for further information.

### D/A CALIBRATION REGISTER 2

BADR3 + 6h

Use InstaCal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond he scope of this document. If you need to program the calibration registers, please contact the factory for further information.

#### D/A 0 - D/A 7 DATA

The following eight registers are the data registers for the eight 16-bit output DACs. D0 is the LSB. Writing to the register will automatically update the DAC output unless the simultaneous update bit is set for that DAC (See the D/A Control Register description for more information on simultaneous update.) The data format is mode-dependent as shown below.

#### **Bipolar Mode:**

Offset Binary Coding

0000h = -FS 8000h = Mid Scale (0V) FFFFh = +FS - 1LSB

#### **Unipolar Mode:**

**Straight Binary Coding** 

0000h = -FS (0V) 8000h = Mid Scale (+FS/2) FFFFh = +FS - 1LSB

#### D/A 0 DATA

BADR3 + 8h

#### WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

#### D/A 1 DATA

BADR3 + 0Ah

# WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

#### D/A 2 DATA

BADR3 + 0Ch

#### WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

### D/A 3 DATA

 $BADR3\ +0Eh$ 

### WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	

# D/A 4 DATA

 $BADR3\ + 10h$ 

# WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

# D/A 5 DATA

BADR3 + 12h

# WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

# D/A 6 DATA

 $BADR3\ +14h$ 

# WRITE ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

## D/A 7 DATA

 $BADR3\ + 16h$ 

## WRITE ONLY

'	11111	OITE	L													
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

# PCI-DDA08/16 PCI-DDA04/16 PCI-DDA02/16

Typical for 25°C unless otherwise specified.

+5V Operating:

PCI-DDA08/16 1.79 A. PCI-DDA04/16 1.65 A. PCI-DDA02/16 1.58 A.

# **Analog Output**

D/A converter type MAX542A Resolution 16 bits

Number of channels:

PCI-DDA08/16 8
PCI-DDA04/16 4
PCI-DDA02/16 2

Output Ranges  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$ , 0 to 10V, 0 to 5V, 0 to 2.5V.

Each channel independently programmable.

#### Data transfer Programmed I/O

Absolute Accuracy (calibrated)

 $\begin{array}{lll} \pm 10 \text{V Range} & \pm 1.18 \text{mV max} \\ \pm 5 \text{V}, 0 \text{ to } 10 \text{V Ranges} & \pm 0.63 \text{mV max} \\ \pm 2.5 \text{V}, 0 \text{ to } 5 \text{V Ranges} & \pm 0.37 \text{mV max} \\ 0 \text{ to } 2.5 \text{V Ranges} & \pm 0.23 \text{mV max} \\ \text{Offset error (calibrated)} & \pm (1 \text{ LSB} + 50 \mu \text{V}) \\ \text{Gain error (calibrated)} & \pm (1.5 \text{ LSBs} + 50 \mu \text{V}) \end{array}$ 

Differential non linearity  $\pm 0.5$  LSBs typ,  $\pm 1$  LSB max. over temperature Integral non linearity  $\pm 0.5$  LSBs typ,  $\pm 1$  LSBs max. over temperature

 $\begin{array}{lll} \mbox{Monotonicity} & 16 \mbox{ bits} \\ \mbox{D/A Gain drift} & \pm 0.1 \mbox{ ppm/°C} \\ \mbox{D/A Unipolar Offset drift} & \pm 0.1 \mbox{ ppm/°C} \\ \mbox{D/A Bipolar Offset drift} & \pm 0.5 \mbox{ ppm/°C} \\ \end{array}$ 

Throughput PC-dependent, 200 kHz max

Settling time (20V step to  $\pm 1.5$  LSBs) 12 $\mu$ s typ, 20 $\mu$ s max

Slew Rate  $2.5V/\mu s$ 

Current Drive ±5 mA

Output short-circuit duration 25 mA; indefinite

Output coupling DC

Output impedance 0.1 Ohms max.

Miscellaneous Double-buffered output latches

Update DACs individually or simultaneously (software-selectable) Power up and reset, all DAC outputs pulled to 0 volts (±3mV

max).

# Digital Input / Output

Digital Type (main connector) 8255 mode 0 emulation

Output: 74S244 Input: 74LS373

Configuration 4 banks of 8, 4 banks of 4,

programmable by bank as input or output

Number of channels 48 I/O

Output High 2.4 volts min @ -15 mA
Output Low 0.5 volts max. @ 64 mA

Input High 2.0 volts min, 7 volts absolute max.
Input Low 0.8 volts max., -0.5 volts absolute min

Power-up / reset state Input mode (high impedance)

# **Environmental**

Operating temperature range 0 to 70°C Storage temperature range -40 to 100°C

Humidity 0 to 90% non-condensing

# **EC Declaration of Conformity**

We, Measurement Computing Corp., declare under sole responsibility that the product:

PCI-DDA0#/16 PCI bus analog output boards with 48-bits of digital I/O
Part Number Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

**EU 55022 Class B**: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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